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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,350	03/21/2000	Steven S. Greenberg	1467-13	6705

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EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	7

DATE MAILED: 01/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,350	GREENBERG, STEVEN S.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 have been presented for Examination. Claims 1-18 have been examined and rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinman U.S. Patent 5,794,005** in view of **"SYMPHONY: A Fast Mixed Signal Simulator for BiMOS Analog/Digital Circuits"** by Premel Buch and Ernest S. Kuh hereafter referred to as the *Buch et al.* reference and in further view of **"NON-INTEGRAL EVENT TIMING FOR DIGITAL LOGIC SIMULATION"** by Ernst G. Ulrich hereafter referred to as the *Ulrich* reference.

2.1 As regards independent **Claim 1** the *Steinman* reference discloses scheduling events in a simulation model for digital circuits **(Figures 1-16),** using hash buckets **(Figures 4 and 5),** organizing the scheduled times into a *priority* heap **(Col. 8 Lines 53-58),** associating

scheduled times assigned to the events in the buckets **(Figure 3, 4, 5, 6, 7, 8, 9, Col. 8 Lines 27-67, Col. 9 Lines 1-51),** removing a earliest scheduled time from the heap **(Figure 14 Items 132, 136 and 110, Col. 10 Lines 49-53),** re-organizing the remaining scheduled times into a new configuration **(Col. 14 Lines 34-54),** and repeating the steps until the queue is empty **(Figure 15 Items 150, 152, 154 and 156).**

However the *Steinman* reference does not expressly disclose events occurring at non-integral times and mixed signaling for mixed analog and digital circuits in a simulation model.

The *Steinman* reference discloses that there is a need in the simulation art to support *multiple simulation strategies* and *other algorithms* **(Col. 17 Lines 46-61).** An artisan of ordinary skill in the art, presented with the problem of simulating a mixed signal integrated circuit would have been motivated to find a method of handling the scheduling of events in a mixed signal circuit simulation. In the related art of mixed signal simulation the *Buch et al.* reference discloses a method of handling event synchronization in a mixed analog and digital circuit simulation **(Page 404 section 2.2 Event Management).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the analog-digital mixed signal simulation event handling technologies of the *Buch et al.* reference because the *Symphony* technology provides a mixed signal simulator for designs with bipolar devices that is efficient **(Buch et al. page 407 Conclusions).**

The *Steinman* reference discloses that there is a need in the simulation art to support *multiple simulation strategies* and *other algorithms* **(Col. 17 Lines 46-61).** An artisan of

ordinary skill in the art, presented with the problem of simulating digital logic would want to have an algorithm that is more efficient. In the same art of digital simulation, the *Ulrich* reference discloses a more efficient method of simulating digital circuits **(pages 61-67).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the non-integral event timing technologies of the *Ulrich* reference because, the *Ulrich* reference teaches a method of reducing un-needed delays as well as removing the possibility of having zero-delay race conditions during the simulation **(page 67).**

2.2 As regards dependent **Claim 2** the *Steinman* reference does not expressly disclose a method of determining events in a mixed signal simulation.

In the related art of analog/digital circuit simulation, the *Buch et al.* reference discloses a method of determining events in a mixed signal simulation **(page 404 Event Management).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the *hash bucket* simulation technologies of the *Steinman* reference with the *event management* technologies of the *Buch et al.* reference because of the improved performance of mixed signal simulations provided by the methods in the *Buch et al.* reference **(page 407).**

2.3 As regards dependent **Claims 3 and 4** the *Steinman* reference teaches the handling of new events **(Figure 13 Item 58).**

3. **Claims 5-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinman U.S. Patent 5,794,005** in view of **"NON-INTEGRAL EVENT TIMING FOR DIGITAL LOGIC SIMULATION"** by Ernst G. Ulrich hereafter referred to as the *Ulrich* reference.

3.1 Regarding independent **Claims 5, 11 and 16** the *Steinman* reference discloses scheduling events for associated scheduled times **(Figures 2 and 11),** and storing the events into buckets **(Figure 3),** and organizing the scheduled times into a structure, wherein the structure is constructed and arraigned to allow easy location of an earliest scheduled time **(Figure 2).**

However, the *Steinman* reference does not expressly disclose non-integral time events.

The *Steinman* reference discloses that there is a need in the simulation art to support *multiple simulation strategies* and *other algorithms* **(Col. 17 Lines 46-61).** An artisan of ordinary skill in the art, presented with the problem of simulating digital logic would want to have an algorithm that is more efficient. In the same art of digital simulation, the *Ulrich* reference discloses a more efficient method of simulating digital circuits **(pages 61-67).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the non-integral event timing technologies of the *Ulrich* reference because, the *Ulrich* reference teaches a method of reducing un-needed delays as well as removing the possibility of having zero-delay race conditions during the simulation **(page 67).**

3.1 As regards dependent **Claim 6** the *Steinman* reference discloses a hash table **(Figures 4 & 5).**

3.2 As regards dependent **Claim 7** the *Steinman* reference discloses a specific scheduled time for events **(Figures 8 & 9).**

3.3 As regards dependent **Claims 8 & 9** the *Steinman* reference discloses a heap **(Col. 8 Lines 53-58).**

3.4 As regards dependent **Claim 10** the *Steinman* reference discloses events, buckets and scheduled times **(Figures 2 & 3).**

3.5 As regards dependent **Claims 11-13** the *Steinman* reference discloses checking to see if the event is done **(Figure 15 Item 152)** and managing event queues **(Figure 1-16).**

3.6 As regards dependent **Claim 15** the *Steinman* reference discloses hash tables **(Figure 3 & 4).**

3.7 As regards dependent **Claim 17** the *Steinman* reference discloses heaps **(Col. 8 Lines 53-58).**

4. Dependent **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinman U.S. Patent 5,794,005** in view of **"NON-INTEGRAL EVENT TIMING FOR DIGITAL LOGIC SIMULATION"** by Ernst G. Ulrich hereafter referred to as the *Ulrich* reference and in further view of **"SYMPHONY: A Fast Mixed Signal Simulator for BiMOS Analog/Digital Circuits"** by Premel Buch and Ernest S. Kuh hereafter referred to as the *Buch et al.* reference.

4.1 As regards independent **Claim 16** see paragraph **3.1** above.

4.2 As regards dependent **Claim 17** the *Steinman* reference does not expressly disclose mixed signal simulation.

The *Buch et al.* reference discloses mixed signal simulation **(Page 404 section 2.2 Event Management).**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have combined the hash bucket scheduling technologies of the *Steinman* reference with the analog-digital mixed signal simulation event handling technologies of the *Buch et al.* reference because the *Symphony* technology provides a mixed signal simulator for designs with bipolar devices that is efficient **(Buch et al. page 407 Conclusions).**

Conclusion

5. **Claims 1-18** have been presented for examination. **Claims 1-18** have been examined and rejected.

5.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- **U.S. Patent 6,324,495** teaches hash-table based event queues used in circuit simulation.
- **U.S. Patent 6,466,898** teaches multi-threaded event management in circuit simulation.
- **U.S. Patent 6,110,217** teaches mixed mode analog/digital circuit simulation.

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100